24. (Amended) A semiconductor wafer [as in claim 11] including:

a plurality of chip sections defined thereon by scribe lines, each chip section having:

bump electrodes formed simultaneously thereon;

a plurality of chip electrodes positioned on said chip section; and

a plurality of interconnection layers for electrically connecting said chip electrodes and said bump electrodes,

said bump electrodes being located at positions other than over said chip electrodes,

wherein each of said interconnection layers comprises an aluminum layer and a plating on said aluminum, wherein said plating contacts said bump electrode and said aluminum layer contacts said chip electrode.

## REMARKS

Claims 5 and 10-28 are pending in the application. Claims 18-22 and 24-27 are indicated to be allowable upon being rewritten in independent form. Therefore, claims 18 and 24 are rewritten in independent form, above, to place claims 18-22 and 24-27 in condition for immediate allowance.

### I. Prior Art Rejections

Claims 5, 10-17, 23 and 28 stand rejected under 35 U.S.C.§ 102(e) as being anticipated by or, in the alternative, under 35 U.S.C. § 103 as obvious over Mori. However, while Applicants submit that the claimed invention is clearly neither anticipated nor rendered obvious by Mori, Applicants note that Mori has a filing date after Applicants' perfected foreign priority date.

Therefore, to expeditiously pass the application to allowance and in order to remove Mori as a valid reference, attached hereto is a verified translation of the priority document. In view of the foregoing, the Examiner is respectfully requested to withdraw these rejections.

## II. Formal Matters

The specification is objected to and claims 5 and 12-17 stand rejected under 35 U.S.C. §112, first paragraph, with respect to the bump and chip electrodes being opposite one another.

In response thereto, Applicants submit that the description regarding the bump and chip electrodes added to the specification clearly does not constitute new matter. However, in order to speed prosecution, the recently added language has been deleted.

Further, with respect to independent claim 5, Applicants submit that the second surface is clearly opposite the first surface. However, again, in order to speed prosecution, and since this is the only remaining issue to place the application in condition for allowance, the offending language (e.g., line 7) has been removed.

Other minor claim amendments have been made to independent claim 5 to compensate for the deletion of the "second layer". Specifically, on lines 9-10, the reference to "second layer" has been removed and the position of the chip electrodes has been defined with respect to the first layer and the wafer. Such a claim amendment does not change the structure defined by the claim. Instead, such amendments merely change the language of the claim to make it acceptable according to the preferences of the Examiner.

In addition, "to" has been added to line 13 of claim 5 to overcome the 35 U.S.C. §112, second paragraph, rejection of claims 5 and 12-17.

Therefore, the Examiner is respectfully requested to reconsider and withdraw this rejection.

## III. No New Issue Is Raised

The foregoing claim amendments clearly do not raise a new issue requiring further consideration and/or search. Specifically, rewriting claims 18 and 24 into independent form merely changes the format of the claims and does not add any new features or change any of the existing features of the claimed invention.

Further, the modifications to claim 5 are made merely to change the language of the claims to make it more acceptable to the Examiner. Such amendments merely change the format of the claims and do not add any new features or change any of the existing features of the claimed invention. Specifically, definition of the location of the chip electrodes is changed from being relative to the second layer to being relative to the first layer and the wafer. Such amendments do not change the claimed structure but merely remove language which the Examiner found objectionable.

Thus, since the foregoing claim amendments do not substantively change the claims, but are made merely to make claims 18 and 24 independent and to resolve informality issues with respect to claim 5, entry of this amendment is proper and requested.

## IV. Conclusion

In view of the foregoing, Applicants submit that claims 5 and 10-28, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is

respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

If any extension of time is required with this document, Applicants hereby make a written conditional petition for extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 23-1951.

Respectfully submitted,

Date : 12/19/97

Frederick W. Gibb, III
Reg. No. 37,629

Whitham, Curtis, Whitham & McGinn
Reston International Center
11800 Sunrise Valley Dr., Suite 900
Reston, Virginia 20191
(703) 391-2510

#13

# TRANSLATOR'S DECLARATION

I, the below-named translator, certify that I am familiar with both the Japanese and the English language, that I have prepared the attached English translation of Japanese document 237653/1994, corresponding to U.S. Application No. 08/533,207, and that the English translation is a true, faithful and exact translation of the corresponding Japanese language document.

I further declare that all statements made in this declaration are believed to be true; and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of legal decisions of any nature based on them.

This 11th day of December, 1997
Date

Name Noriyasu Ikeda

(Translation)

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this Office.

Date of Application: The 30th day of September, 1994

Application Number: Patent Application No. 237653 of the year of Heisei 6 (1994)

Applicant(s): NEC Corporation

This 4th day of August, 1995

Commissioner,
Patent Office Yuji Kiyokawa

Certificate No. P-Hei-07-3042783

(Translation)

[Name of Document] SPECIFICATION

[Title of Invention] PROCESS FOR MANUFACTURING A SEMICONDUCTOR DEVICE AND A SEMICONDUCTOR WAFER

[Claim for Patent]

[Claim 1] A process for manufacturing a semiconductor device, comprising:

a step of forming on a wafer a plurality of semiconductor chip regions each of which region has a plurality of electrode pads along a periphery thereof, an entire surface of said wafer being covered with a passivation film except said plurality of electrode pads;

a step of forming on said wafer a plurality of interconnections for each of said plurality of semiconductor chip regions so that said interconnections have one ends connected to said plurality of electrode pads, respectively, and are extended inward of said semiconductor chip regions;

a step of covering the entire surface of said wafer with a cover coating film;

a step of forming a plurality of openings in said cover coating film in a matrix pattern;

a step of forming a plurality of bumps on said plurality of openings, respectively; and

a step of separating said plurality of semiconductor chip regions formed on said wafer into individual semiconductor chips along scribe lines.

(Translation)

[Name of Document] Patent Application

[Reference Number] J-1081

[Filing Date] September 30, 1994

[To] Commissioner, Patent Office

[International Class] H01L 21/60

[Title of Invention] Process For Manufacturing A Semiconductor Device And A Semiconductor Wafer

[Number of Claim(s)] 5

[Inventor]

[Address] c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo

[Name] Keiichiro Kata

[Inventor]

[Address] c/o NEC Corporation, 7-1, Shiba 5-chome, Minato-ku, Tokyo

[Name] Shinichi Chikaki

[Applicant]

[Identification Number] 000004237

[Name] NEC Corporation

[Representative] Hisashi Kaneko

[Attorney]

[Identification Number] 100071272

[Patent Attorney]

[Name] Yosuke Goto

[Appointed Attorney]

[Identification Number] 100077838

[Patent Attorney]

[Name] Noriyasu Ikeda

[Appointed Attorney]

[Identification Number] 100058413

[Patent Attorney]

[Name] Hiroshi Ashida

[Official Fee]

[Payment] Deposit

[Deposit Number] 012416

[Sum] 21000

[List of Presented Documents]

[Name] Specification 1

[Name] Drawing 1

[Name] Abstract 1

[Registration Number of General Power of Attorney] 9001569

[Proof] Required.

[Claim 2] A process for manufacturing a semiconductor device as claimed in claim 1, wherein said interconnections extended inward of said semiconductor chip regions are formed so as to be exposed through said plurality of openings.

[Claim 3] A process for manufacturing a semiconductor device as claimed in claim 1, wherein said bumps are formed away from said scribe lines.

[Claim 4] A process for manufacturing a semiconductor device as claimed in claim 1, wherein said bumps are formed away from said electrode pads.

[Claim 5] A semiconductor wafer including a number of said semiconductor chips, wherein matrix bump electrodes are formed on an entire surface of said wafer except scribe lines between said semiconductor chips.

[Detailed Description of the Invention]

[0001]

[Industrial Application Field]

This invention relates to a process for manufacturing a semiconductor device and, in particular, to a process for manufacturing a semiconductor device suited for high packaging density.

[0002]

[Prior Art]

Semiconductor packages of various new forms have been developed in order to meet demands such as reduction in size and weight, increase in speed, and improvement in function of electronic devices. Demands for increase in

number of pins following development of a highly integrated semiconductor chip (simply called a chip hereinafter) and for reduction in size and thickness of the device become severe. In order to simultaneously meet those demands, fine pitch arrangement is inevitably required. Therefore, it is expected that inner lead bonding capable of narrowing the pitch and area array bonding capable of widening the pitch will become essential techniques.

[0003]

Presently, a wire bonding technique is mainly used for electrical connection between the chip and a lead, i.e. so-called inner lead bonding (ILB). The wire bonding technique herein referred to is to connect bonding pads on the chip and leads on the package by the use of fine wires having a diameter from 20 to 30 $\mu$m. The wire bonding technique includes thermo compression bonding, ultrasonic bonding, and thermosonic bonding combining their characteristics.

[0004]

However, following the increase in number of the pins, the pad pitch is narrowed so that the connection is difficult. Under the circumstances, attention is directed to a wireless bonding technique instead of the wire bonding technique. The wireless bonding technique is a method in which all electrode pads (simply called pads hereinafter) on the chip are simultaneously bonded to terminals on the package by specific bumps or metal

leads, and is also called gang bonding. The wireless bonding technique includes TAB (tape automated bonding) and flip chip.

[0005]

In the TAB technique, an inner lead of metal foil formed by etching on an insulating film is bonded to the bumps formed on an electrode pad of the chip. Thus, the technique is advantageous in achieving a reduced thickness and compact packaging. The TAB technique is also called a tape carrier technique. On the other hand, the flip chip technique is a method in which a solder bump is formed on an active element surface of the chip and the chip is reversed and directly connected to a substrate. Thus, this technique is adapted for the increase in number of pins and the reduction in pitch. Furthermore, the length of interconnection is extremely short so that this technique is also advantageous for increase in speed and reduction in noise.

[0006]

Either of the TAB technique and the flip chip technique uses the bumps provided between the chip and the film (package) to make electrical connection therebetween. These techniques are disclosed in, for example, Japanese Unexamined Patent Publications Nos. 129366/1993 and 77293/1994.

[0007]

Furthermore, the present applicant has proposed a novel technique, which is one of the wireless bonding

techniques, for electrical connection between the semiconductor chip and the carrier film (Japanese Patent Application No. 110857/1994 filed on May 25, 1994, entitled "FLEXIBLE FILM AND SEMICONDUCTOR DEVICE COMPRISING THE SAME"). In the novel technique, the bumps are not used for the electrical connection between the chip and the carrier film. The bumps are formed on the surface of the carrier film on which the chip is not mounted.

[0008]

Now referring to Fig. 3, description will be made about a conventional manufacturing process, which is disclosed in the above-mentioned Japanese Unexamined Patent Publication No. 110857/1994, of manufacturing a film carrier semiconductor device in which the semiconductor bare chip and the carrier film are electrically connected during the assembling process.

[0009]

At first, necessary materials required to form the film carrier semiconductor device are the semiconductor bare chip 10, the carrier film 20, and an adhesion film 30, as shown in Fig. 3(A).

[0010]

The carrier film 20 comprises a polyimide-based organic insulation film 21. On one principal surface of the insulation film 21, an interconnection layer 22 having connecting portions to the semiconductor bare chip 10 is formed. Furthermore, through holes are formed in

the insulation film 21. One end of each through hole is adjacent to the interconnection layer 22 at a portion different from the connecting portions while the other end reaches a back surface of the insulation film 21. The through hole is filled with a conductive electrode 23. Openings are formed in the insulation film 21 at portions corresponding to the connecting portions of the interconnection layer 22. A filling material 24 is inserted in each opening. For the detailed structure of the carrier film 20 and the manufacturing process thereof, see the above-mentioned Japanese Patent Application No. 110857/1994.

[0011]

The adhesion film 30 is cut into a size smaller than a chip size and has a thickness on the order of several tens of microns.

[0012]

As shown in Fig. 4, the semiconductor bare chip 10 is prepared by forming a large number of chip regions on a wafer 40 by the use of a well-known wafer manufacturing technique and separating these regions into individual chips by dicing along scribe lines 13. In general, the dicing is carried out using a dicing saw. In the semiconductor bare chip 10 shown in the figure, electrode pads 11 are arranged along the periphery of the chip but may be located in an active region. An aluminum-based alloy is generally used as a metal material forming the electrode pads 11. On the other hand, a polyimide

film, a silicon nitride film, and a silicon oxide film, and the like are used as a passivation film 12 formed on the surface of the semiconductor bare chip 10.

[0013]

Turning to Fig. 3(B), the adhesion film 30 which has been cut as described above is accurately positioned and set on the semiconductor bare chip 10. If thermoplastic resin is used as the adhesion film 30, the adhesion film 30 can be temporarily fixed by heating from the side of the semiconductor bare chip 10 up to a temperature at which the adhesion film 30 is melted. In this event, the adhesion film 30 must be set and heated in a manner such that no voids are trapped.

[0014]

Turning to Fig. 3(C), the carrier film 20 and the semiconductor bare chip 10 with the adhesion film 30 temporarily fixed thereon are positioned relative to each other by the use of a single-point bonder used in the connection by the TAB technique. Thereafter, inner lead connection is carried out. The bonding becomes strong by alloying of aluminum forming the electrode pads 11 of the semiconductor bare chip 10 and copper forming the interconnection layer 22 of the carrier film 20.

[0015]

Next, turning to Fig. 3(D), in order to adhere the carrier film 20 and the semiconductor bare chip 10 with the adhesion film 30 interposed therebetween, heating and pressurizing are carried out for several

seconds from the the side of the carrier film 20 or the semiconductor bare chip 10. As a consequence, the carrier film 30 and the semiconductor bare chip 10 are adhered to each other.

[0016]

On the other hand, the adhesion of the carrier film 20 and the semiconductor bare chip 10 is not restricted to the manner illustrated in Figs. 3(B)-(D). For example, the adhesion film 30 may be set on the carrier film 20. The inner lead connection may be carried out after the carrier film 20 and the semiconductor bare chip 10 are adhered with high positional accuracy with the adhesion film 30 interposed therebetween. Alternatively, an adhesion layer may preliminarily be formed on the surface of the chip in the wafer stage.

[0017]

Next, in Fig. 3(E), electrical sorting and BT are carried out by the use of a sorting pad 25 in the manner similar to that for a typical tape carrier package (TCP). By designing the outer configuration and the size of the carrier film 20 in accordance with EIAJ, sorting tools such as sockets and balls can be used in common.

[0018]

Turning to Fig. 3(F), a product name is labelled on a back surface of the chip by laser marking. Thereafter, the cutting of outer configuration is carried out using a die. Taking into account the cutting margin,

cutting is generally carried out into a size larger by about 100$\mu$m on each side. Cutting with high accuracy can be carried out by using a dicing saw and a laser.

[0019]

Finally, turning to Fig. 4(G), solder bumps 26 are formed on outer connection pads arranged on the substrate-side surface of the carrier film 20 in a matrix pattern at the constant pitch. The solder bumps 26 can be formed, for example, by the process disclosed in Japanese Unexamined Patent Publication No. 52973/1974. Specifically, using the wire bonding technique, a solder wire is formed into a ball. After the ball is adhered onto each pad, the wire except the ball is cut off. Through the above-mentioned process, the film carrier semiconductor device is completed.

[0020]

In the meanwhile, there are various kinds of semiconductor devices. Among others, a memory and a liquid crystal drive are suitable for mass production. Considering application to such kinds of products, the above-mentioned manufacturing process in which the semiconductor bare chip 10 and the carrier film 20 are electrically connected during the assembling process is disadvantageous because mass production of semiconductor devices is difficult. In view of the above, a batch process in which operations are conducted on the wafer is believed to be effective for mass production of the semiconductor devices.

[0021]

Such batch process in which the bumps are formed on the wafer 40 is known. This process is a technique developed by IBM and is called a C4 technique. In this technique, a barrier metal is formed on Al electrode pads (chip electrodes) and solder bumps are deposited thereon by vapor deposition.

[0022]

[Problem to be solved by the Invention]

As described above, the bumps are formed on the wafer. In this case, however, since the electrode pads 11 of the semiconductor chip 10 are arranged at the periphery of the chip, the bumps on the wafer are essentially formed on each pad in correspondence to the electrode pads on the chip. On the other hand, it is also proposed to arrange the electrode pads of the chip throughout the entire surface of the chip. For this purpose, however, a multi-layered electrode structure must be adopted which allows the arrangement of the pads throughout the entire surface. This structure is disadvantageous because the manufacture is difficult and surface flatness is greatly affected. Furthermore, in order to simultaneously achieve shrinkage of the chip size and the increase in number of pins, the pitch of the electrode pads becomes narrower. Therefore, it is practically difficult to form or mount the solder bumps at positions corresponding to the electrode pads. Moreover, even if it is tried to solve the above

difficulty by means of the multi-layered structure, it is obvious that the difficulty in manufacture is encountered as described above.

[0023]

On the other hand, the above-mentioned manufacturing process in which the semiconductor bare chip 10 and the carrier film 20 are electrically connected during the assembling process after separation of the chips is disadvantageous in view of the reliability of the connecting portion between the semiconductor bare chip 10 and the carrier film 20. Furthermore, another problem may arise about the tight contact at the interface between the semiconductor bare chip 10 and the carrier film 20.

[0024]

Accordingly, an object of this invention is to provide a process capable of mass-producing semiconductor devices having bumps formed at different positions from electrode pads.

[0025]

Another object of this invention is to provide a process for manufacturing a semiconductor device having an excellent T/C resistance.

[0026]

Still another object of this invention is to provide a process for manufacturing a semiconductor device having an excellent moisture resistance.

[0027]

[Means to solve the Problem]

According to this invention, there is provided a process for manufacturing a semiconductor device, comprising a step of forming on a wafer a plurality of semiconductor chip regions each of which region has a plurality of electrode pads along a periphery thereof, an entire surface of the wafer being covered with a passivation film except the plurality of electrode pads; a step of forming on the wafer a plurality of interconnections for each of the plurality of semiconductor chip regions so that the interconnections have one ends connected to the plurality of electrode pads, respectively, and are extended inward of the semiconductor chip regions; a step of covering the entire surface of the wafer with a cover coating film; a step of forming a plurality of openings in the cover coating film in a matrix pattern; a step of forming a plurality of bumps on the plurality of openings, respectively; and a step of separating the plurality of semiconductor chip regions formed on the wafer into individual semiconductor chips along scribe lines.

[0028]

In the above-mentioned process for manufacturing a semiconductor device, the interconnections extended inward of the semiconductor chip regions are preferably formed so as to be exposed through the openings. Furthermore, the bumps are preferably formed away from the scribe lines. In addition, the bumps are preferably

formed away from the electrode pads.

[0029]

According to this invention, there is also provided a semiconductor wafer including a number of the semiconductor chips, wherein matrix bump electrodes are formed on an entire surface of the wafer except scribe lines between the semiconductor chips.

[0030]

[Embodiment]

Now, this invention will be described with reference to the drawing.

[0031]

Fig. 1 shows process for manufacturing a semiconductor device according to one embodiment of this invention. At first, as shown in Fig. 1(A), a plurality of semiconductor chip regions are formed on the wafer 40 by the use of a well-known wafer manufacturing process. Each of the semiconductor chip regions has a plurality of electrode pads 11 along a periphery thereof.

[0032]

Next, turning to Fig. 1(B), the wafer 40 is coated with a passivation film 12 by spin coating. The passivation film 12 has a thickness not greater than 20$\mu$m. Next, the plurality of electrode pads 11 are formed by means of well-known exposing and etching techniques. Thus, an entire surface of the wafer 40 except the plurality of electrode pads 11 is covered with the passivation film 12. This wafer 40 is shown in Fig.

4. As described above, in the conventional technique, the plurality of semiconductor chip regions formed on the wafer 40 are separated into individual semiconductor bare chips by dicing along the scribe lines 13. In this invention, dicing is not yet carried out in this stage.

[0033]

Turning to Fig. 1(C), a plurality of Al interconnections 14 are formed on the wafer 40 for each of the plurality of semiconductor chip regions so that this interconnections have one ends connected to the plurality of electrode pads and are extended inward of the semiconductor chip regions. The formation of the Al interconnections 14 is carried out using a mask by means of a thin-film deposition technique such as sputtering. The Al interconnections 14 have a thickness not greater than 1$\mu$m.

[0034]

Turning to Fig. 1(D), an Ni plating layer 15 is formed on the Al interconnections 14. Instead of the Ni plating layer 15, use may be made of other metals, for example, Cu plating capable of being barrier metal of a solder bump. The Ni plating layer essentially has a thickness at least on the order of 5$\mu$m in order to secure reliability of the solder connecting portion and to absorb thermal stress resulting from a difference in thermal expansion between the chip and the packaging substrate. In this embodiment, the Ni plating layer 15 has a thickness on the order of 10$\mu$m.

[0035]

Turning to Fig. 1(E), the entire surface of the wafer 40 is covered with a cover coating film 16. The cover coating film 16 is made of, for example, polyimide and has a thickness not greater than 20$\mu$m. Subsequently, a plurality of openings 17 are formed in the cover coating film 16 in a matrix pattern at positions where solder bumps which will later be described are to be formed. The formation of the openings 17 is carried out by means of etching or laser processing. The surface of the Ni plating layer 15 is exposed through the openings 17. The surface of the Ni plating layer 15 thus exposed is subjected to Au plating. This aims to suppress a defective ratio upon formation of the solder bumps which will later be described.

[0036]

Turning to Fig. 1(F), a plurality of the solder bumps 18 are formed in the plurality of openings 17, respectively. The solder bumps (bump electrodes) 18 has a height on the order of 100$\mu$m. The solder bumps 18 can be formed, for example, by means of the following process. At first, a solder piece is formed by punching a solder ribbon by the use of a combination of a die and a punch. Next, the solder piece is adhered in each opening 17 using an adhesive material such as flux. Finally, the solder bumps 18 are formed by heat treatment and by washing out the flux.

[0037]

The wafer 40 at this state is shown in Fig. 2. As shown in Fig. 2, the matrix bump electrodes 18 are formed on the entire surface of the wafer 40 except the scribe lines 13 between the semiconductor chips. The Al interconnections 14 extended inward of the semiconductor chip regions are arranged so as to pass through the plurality of openings 17. The bump electrodes 18 are formed away from the scribe lines 13. Furthermore, the bump electrodes 18 are formed away from the electrode pads 11.

[0038]

Finally, turning to Fig. 1(G), the plurality of semiconductor chip regions formed on the wafer 40 are separated into individual semiconductor chips 10 by dicing along the scribe lines 13.

[0039]

In the conventional wafer 40 shown in Fig. 4, the electrode pads 11 are arranged at a pitch on the order of 0.1mm. On the other hand, the pitch of the bump electrodes 18 can be widened up to about 0.5mm in the wafer shown in Fig. 2. Thus, during the formation of the solder bumps 18 in Fig. 1(F), occurrence of short-circuiting defect between the bump electrodes can be dramatically reduced. Furthermore, the yield is also improveed upon packaging on the packaging substrate. In addition, there is another advantage that standardization is easy. Furthermore, bonding strength between the solder bumps 18 and the Ni plating layer 15 is high.

[0040]

Although this invention has been described in conjunction with the embodiment, it will readily be understood that this invention is not limited to the above embodiment but various changes and modifications may be made within a range not departing from the scope and spirit of this invention. For example, Au bumps may be used as the bumps instead of the solder bumps. In this case, the step of forming the Ni plating layer 15 and the Au plating process can be eliminated.

[0041]

[Effect of the Invention]

As described above, according to this invention, the electrode pads formed at the periphery of each semiconductor chip region are led to the inside and the bump electrodes are rearranged in a matrix pattern. Thus, it is possible to mass-produce the semiconductor devices. Furthermore, a new investment is unnecessary because this process is an extension of the conventional chip manufacturing process. In addition, this invention removes a problem in prior art as to the reliability of the connecting portion between the semiconductor bare chip and the carrier film and has an excellent T/C resistance. Furthermore, the tight contactness at each interface is high so that the moisture resistance is excellent.

[Brief Description of the Drawing]

[Fig. 1]

A sectional view showing a process for manufacturing a semiconductor device according to one embodiment of this invention.

[Fig. 2]

Views showing a semiconductor wafer relating to this invention, (a) being a plan view, (b), an enlarged view of an encircled part in (a), (c), a sectional view taken along a line B-B' in (b).

[Fig. 3]

A sectional view showing a conventional process for manufacturing a semiconductor device.

[Fig. 4]

Views showing a conventional semiconductor wafer, (a) being a plan view, (b), an enlarged view of an encircled part in (a), (c), a sectional view taken along a line A-A' in (b).

[Description of Reference Numerals]

10 a semiconductor chip

11 an electrode pad

12 a passivation film

13 a scribe line

14 an Al interconnection

15 an Ni plating

16 a cover coating film

17 an opening

18 a solder bump (bump electrode)

40 a wafer

[Name of Document] ABSTRACT

[Abstract]

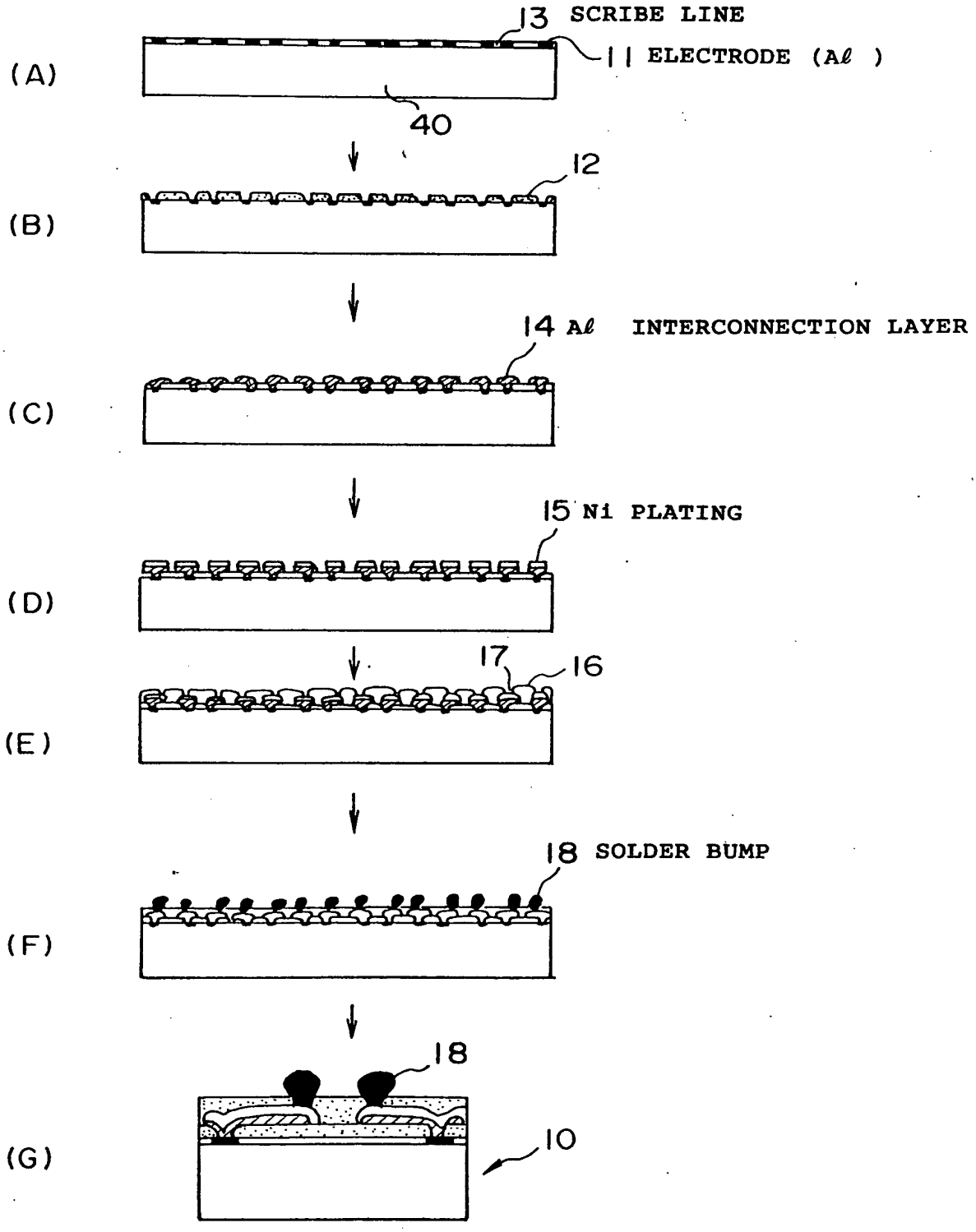
[Object] To mass-produce semiconductor devices which have high reliability of connecting portions and high tight contactness at every interface.

[Structure] On a wafer 40, a plurality of semiconductor chip regions are formed. Each of the semiconductor chip regions has a plurality of electrode pads 11 along a periphery thereof and an entire surface of the wafer is covered with a passivation film 12 except the plurality of electrode pads. On the wafer, a plurality of interconnections 14 are formed for each of the plurality of semiconductor chip regions so that the interconnections have one ends connected to the plurality of electrode pads, respectively, and are extended inward of the semiconductor chip regions. The entire surface of the wafer is covered with a cover coating film 16. A plurality of openings 17 are formed in the cover coating film in a matrix pattern. A bump 18 is formed at each openings. The semiconductor chip regions formed on the wafer are separated into individual semiconductor chips along scribe lines 13.

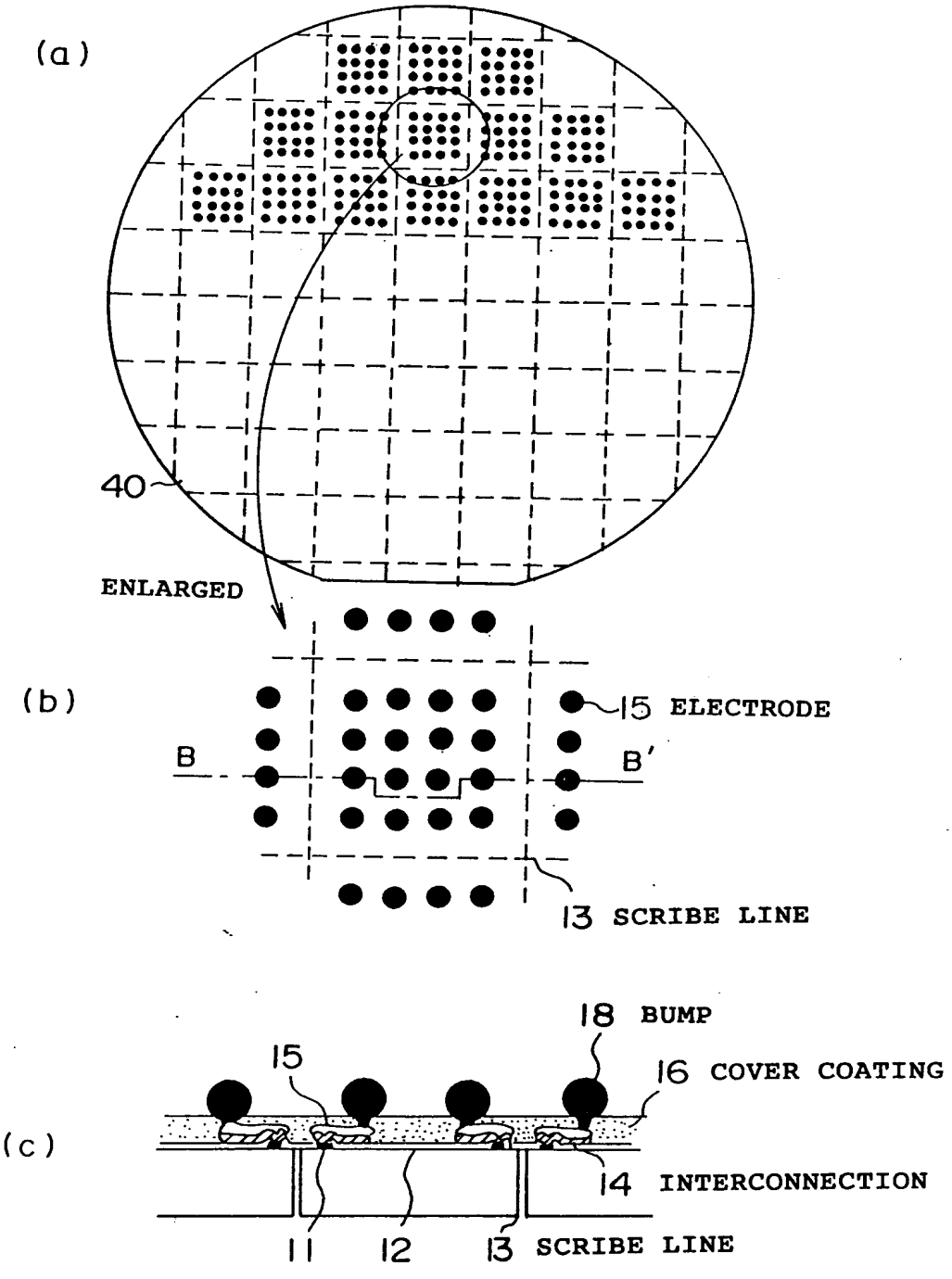
[Selected Figure] Fig. 1

[NAME OF DOCUMENT] DRAWING

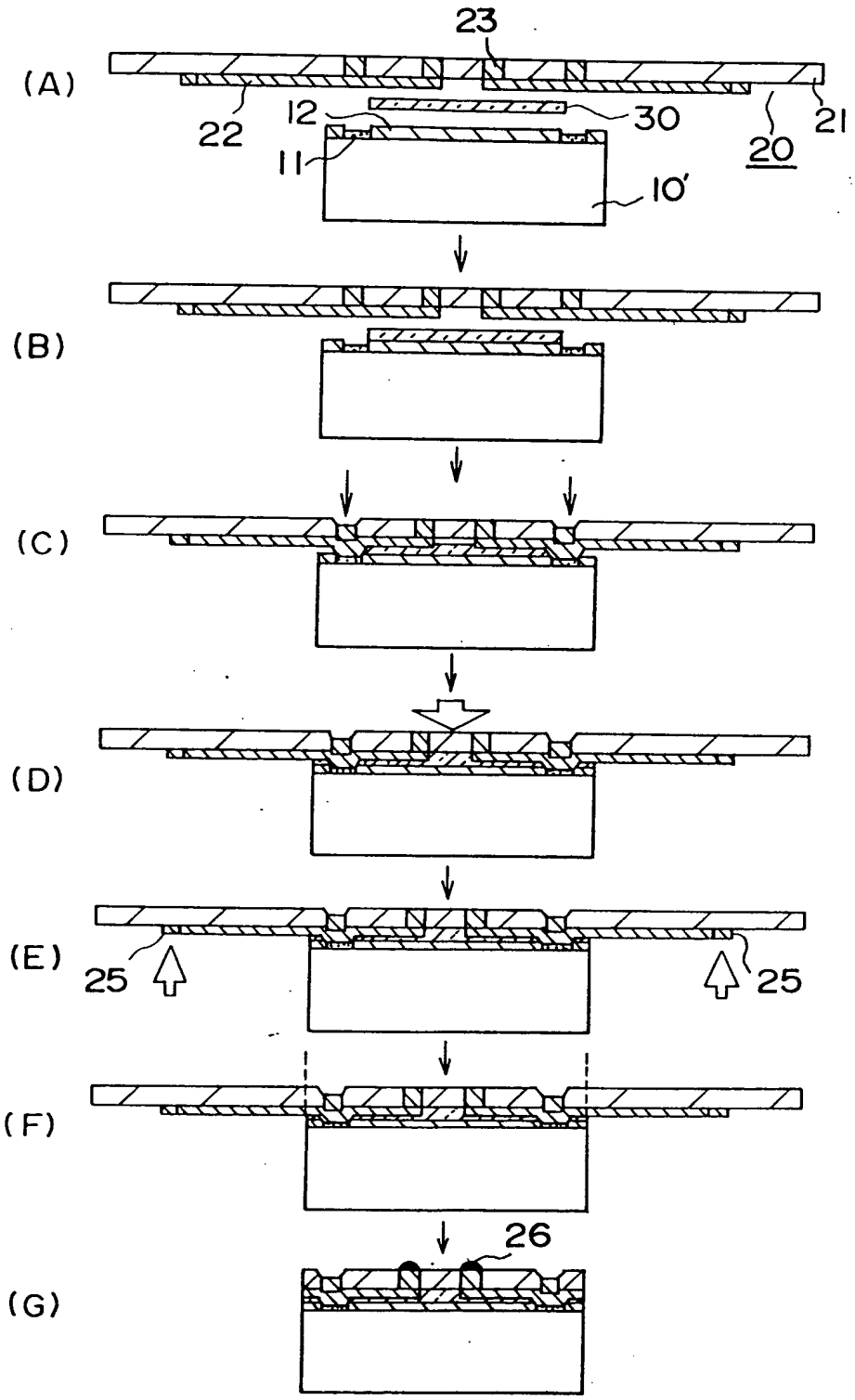
[FIG. 1]



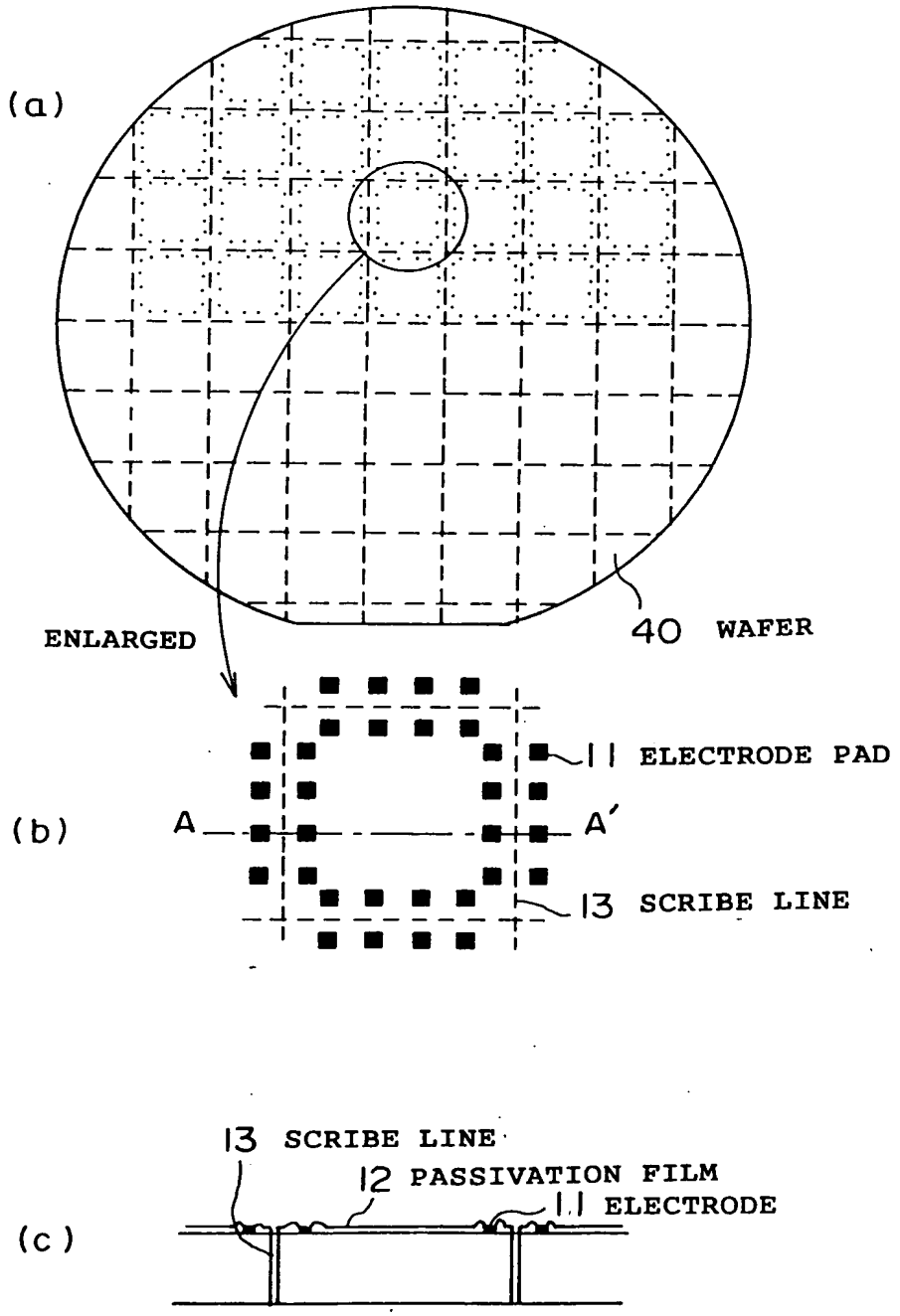
[FIG. 2]


(a)
40
ENLARGED
(b)
15 ELECTRODE
B
B'
13 SCRIBE LINE
(c)
18 BUMP
15
16 COVER COATING
14 INTERCONNECTION
11
12
13 SCRIBE LINE

[FIG. 3]



[FIG. 4]


(a)
ENLARGED
40 WAFER
11 ELECTRODE PAD
(b)
A
A'
13 SCRIBE LINE
13 SCRIBE LINE
12 PASSIVATION FILM
11 ELECTRODE
(c)